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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, May 2015
(2013 Scheme)
13.402 : DIGITAL ELECTRONICS AND LOGIC DESIGN(E)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** quesion carries **two** marks. **(10×2=20 Marks)**

1. State commutative laws of Boolean algebra.
2. State Demorgan's theorem.
3. Convert 145 to BCD, excess 3 and gray code.
4. Draw half adder circuit with truth table.
5. List out advantage and disadvantage of major logic families.
6. Draw logic diagram and truth table of clocked SR flip-flop.
7. What is state diagram ?
8. Draw monostable using logic gates.
9. Draw the basic structure of RAM.
10. What is VHDL ?

PART – B

Answer **any one full** question from **each** Module. **(4×20=80 Marks)**

Module – I

11. a) Plot Boolean expression $Y = \overline{A}\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D$ on the karnaugh map. 10

    b) Plot Boolean expression $Y = (A + B + C + \overline{D})\,(A + \overline{B} + \overline{C}\,D)\,(\overline{A} + \overline{B} + C + \overline{D})\,(\overline{A} + \overline{B} + \overline{C} + D)$. 10

OR

12. Minimize the expression using quine McCluskey method.
    $Y = \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,\overline{D}$. 20

Module – II

13. a) Design 1 : 8 de-multiplexer using two 1 : 4 de-multiplexer. 10

    b) Implement 4 bit adder/subtractor using logic gates. 10

OR

14. Explain BCD to seven segment decoder with logic diagram. 20

Module – III

15. a) Explain with diagram and wave form JK flip-flop to D flip-flop. 10

    b) With diagram and waveform describe 4 bit SIPO shift register. 10

OR

16. a) With diagram and wave form explain 4 bit ripple counter. 10

    b) Describe with diagram and wave form 4 bit Johnson counter. 10

Module – IV

17. With diagram explain 4 bit PROM organization. 20

OR

18. Describe principle of operation of 555 timer astable multivibrator circuit with a circuit diagram and internal block diagram. 20